

[illegible]

The diagram shows a 5V DC input connected to the VIN pin of an HT7833 voltage regulator (U1). The VOUT pin is connected to a 3.3V output, which is also connected to the VDD pin of the microcontroller (elink32). A 10µF capacitor (C5) is connected between VIN and GND, and another 10µF capacitor (C6) is connected between VOUT and GND. The GND pin of the regulator is connected to the common ground of the circuit.

The diagram shows the B8 module connected to the U3 MX25L8006E (NC) USON_4x4 flash memory. The B8 module is connected to PA10 IAP and B8 IAP(NC) KEY2-SMT. The U3 flash memory is connected to VDD_elnk32, Flash CS, Flash MISO, Flash SCK, Flash MOSI, and GND. A 10K(NC) 0603-R resistor is connected between VDD_elnk32 and Flash CS. A 0.1uF(NC) 0603-C capacitor is connected between VDD_elnk32 and Flash SCK.

**Designator Reserved For Target Board as below,
Do NOT Use in this sheet:**

- B1 to B7**
- C14 to C50**
- CN4 to CN7**
- D5 to D50**
- J1 to J7**
- R11 to R50**
- S1 to S7**
- U7 to U20**
- X1 , Y2**

CN8
Virtual COM Port
HDR1X3

— CN8

DAP RX
DAP TX

R56 100 0603-R

R51 100 0603-R

GND


VDD_elink32 J8 HDR1X2 VDD_TargetBoard

J8: VDD Option
Short : Output
Open : Input

GND C13 9.1uF 0603-C U5 1 2 3 4 5 6 VCCA VCCB GND DIR1 DIR2 SWDIO MOSI MISO R9 470 0603-R SN74LVC1T45 SOT23-6

VDD_elink32 VDD_TargetBoard

GND C51 9.1uF 0603-C U6 1 2 3 4 5 6 VCCA VCCB GND DIR1 DIR2 SWDIO SCK SWCLK SN74LVC1T45 SOT23-6

The name of PCB *	Size HT A4	
Title e-Link32 Lite CMSIS DAP	Rev. V2.3	
Date: 2017/7/12 File: e-link32 Lite V2.3.SchDoc	Sheet 1 of 2 Drawn By: Chien	